**Department offering the program:** Electronics and Electrical Communications Engineering
**Department offering the course:** Electronics and Electrical Communications Engineering

# Course Specification

| 1. **Course Basic Information** | | |
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| **Code ECE 212**<br>**Department requirement** | **Title:** Very Large Scale Integrated Circuit | **Academic year:** 2015-2016<br>**Level** (2) – **Semester** ($1^{st}$) |
| **Field: Basic Eng. Science** | **Teaching hours:** Lecture [2] Tutorial [1] Lab [0] | |

| 2. **Course Objectives** | 1. To provide students with the basics of MOS transistor theory and modeling using SPICE.<br>2. To give students a comprehensive study for the principles and techniques of modern VLSI systems design.<br>3. To develop the student's skills to analyze and design the VLSI technology.<br>4. To teach students the analysis of combinational MOS logic circuits, sequential MOS logic circuits, and MOS semiconductor memories.<br>5. To equip students with integrated circuits different fabrication methods. |
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| **3. Intended learning outcomes: ARS** | | **Course ILOs** |
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| **A- Knowledge and understanding** | A.1 Explain concepts and theories of mathematics and science, appropriate to very large scale integrated circuit. | A.1.1 Explain MOS transistors concepts and theories.<br>A.1.2 Explain VLSI layout concepts.<br>A.1.3 Explain the concepts of inverter, static and dynamic logic, and memory circuits. |
| | A.3 Describe characteristics of engineering materials related to very large scale integrated circuit. | A.3.1 Describe characteristics of materials used in integrated circuit fabrication. |
| | A.4 Demonstrate principles of design including elements design, process and/or a system related to very large scale integrated circuit. | A.4.1 Demonstrate design principles of combinational and sequential MOS logic circuits.<br>A.4.2 Demonstrate design principles of MOS semiconductor memories. |
| | A.8 Describe current engineering technologies as related to very large scale integrated circuit. | A.8.1 Describe current engineering technologies related to MOS logic circuits.<br>A.8.2 Describe current engineering technologies related to MOS semiconductor memories.<br>A.8.2 Describe current engineering technologies related to integrated circuits fabrication. |
| | A.19 Explain methods of fabrication of integrated circuits. | A.19.1 Describe methods of fabrication of MOS semiconductor memories.<br>A.19.1 Describe methods of fabrication of combinational and sequential MOS logic circuits. |

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| **B- Intellectual skills** | B.1 Select appropriate mathematical and computer-based methods for modeling and analyzing problems. | B.1.1 Select appropriate mathematical methods for analyzing MOS transistor performance.<br>B.1.2 Select appropriate computer-based methods for modeling MOS transistor using SPICE. |
| | B.5 Assess and evaluate the characteristics and performance of components, systems and processes. | B.5.1 Assess the characteristics of static and dynamic inverters.<br>B.5.2 Evaluate the performance MOS transistor. |
| | B.6 Investigate the failure of components, systems, and processes. | B.6.1 Investigate the failure of MOS semiconductor memories. |
| **C- Professional skills** | C.2 Professionally merges the engineering knowledge, understanding, and feedback to improve design, products and/or services. | C.2.1 Professionally merges the engineering knowledge and understanding to improve MOS semiconductor memories design. |
| | C.3 Create and/or re-design a process, component or system, and carry out specialized engineering designs. | C.3.1 Create combinational and sequential MOS logic circuits.<br>C.3.2 Create MOS semiconductor memories circuits.<br>C.3.3 Create layout designs for different integrated circuits. |
| | C.6 Use a wide range of analytical tools, techniques, and software packages pertaining to very large scale integrated circuits and develop required computer programs. | C.6.1 Use SPICE analytical tool for modeling MOS transistors.<br>C.6.2 Use the appropriate software package to make VLSI layout. |
| **D- General skills** | D.2. Work in stressful environment and within constraints. | D.2.1 Work in stressful environment and within constraints in understanding Modeling of transistor using SPICE. |
| | D.3 Communicate effectively. | D.3.1 Communicate effectively, in class room and lab time with his colleagues and staff members. |
| | D.4 Demonstrate efficient IT capabilities. | D.4.1 Demonstrate efficient IT capabilities with using SPICE. |
| | D.6 Effectively manages tasks, time, and resources. | D.6.1 Effectively manages tasks, time, and resources in the Lab assignments, and exams. |

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| | D.7. Search for information and engage in life-long self learning discipline. | D.7. 1 Search for information and engage in life-long self learning in modeling of MOS transistor and fabrication of MOS circuits.<br>D.7. 2 Search for information and engage in life-long self learning relevant to integrated circuits analysis and design. |
| 4. **Course contents** | MOSFET and Fabrication Technology, The pass transistor, NMOS, MOS Inverter and BiCMOS. Fabrication of NMOS Device/ Transistor Fabrication of CMOS Devices, n-Well Process, P-well Processing Steps Twin-Tub Processing. Stick diagrams. NMOS design style, CMOS-design style. Design rules and layout, Lambda-based design rules. Double metal MOS process rules, CMOS lambda-based design rules, 2µm double metal, double poly. CMOS / BiCMOS rules, Layout diagrams, Symbolic diagrams - translation to mask form. Transmission gates, Gate (restoring) logic. The inverter, Two-input NMOS, CMOS and BiCMOS Nand gates, Two-input nMOS, CMOS and BiCMOS Nor gates. Pseudo-nMOS logic, Dynamic CMOS logic, Clocked CMOS (CZMOS) logic, CMOS domino logic, n-p CMOS logic, A parity generator, Bus arbitration iogic for n-line bus. Multiplexers (data selectors), A general logic function block, A four-line Gray code to binary code converter, The programmable logic array (PLA), Two-phase clocking, Charge storage, Dynamic register element, A dynamic shift register. Illustration of the design process computational elements, Some observations on the design process, Design of a 4-bit adder, Implementing ALU functions with an adder, The Manchester carry-chain. Some CMOS design projects, CMOS project 1 - an incrementer/decrementer: MOS project 2 - left/right shift serial/para register: CMOS project 3 - a comparator for two n-bit numbers: CMOS/BiCMOS project 4 - a two-phase non-overlapping clock generator with buffered output on both phases: CMOS project 5 - design of a latch - an event-driven latch element for EDL systems.<br>**ترانزستور تأثير المجال ذو البوابة المعزولة و طرق تصنيعه- عاكس ترانزستور تأثير المجال ذو البوابة المعزولة - دوائر العاكس المتكامل و ثنائى القطبية- التصنيع باستخدام البئرالالكترونى و التصنيع باستخدام البئر الفجوى- الرسم التخطيطى للترانزستور- قواعد الرسم التخطيطى للتصميم- التحويل لصورة القناع- بوابات النقل – البوابات المنطقية- دوائر النانـد و النور- المولد الازدواجى- الدامجات – تحويلات الجراى كود- مصفوفات البوابات المبرمجة- المسجلات الديناميكية- تصميم العناصر الحسابية المجمعة- تصميم الجامع – تصميم الوحدات الحاسبة و المنطقية- مشاريع تطبيقية.** |
| **5. Teaching and learning methods** | - Lectures<br>- Tutorials<br>- Labs and case studies<br>- Research assignments |
| **6. Teaching and learning methods for disable students** | - Assign a portion of the office hours for those students.<br>- Arrange meetings for more discussion and declaration.<br>- Repeat the explanation of some of the material and tutorials.<br>- Assign a teaching assistance to follow up the performance of this group |

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| | of students. |
| **7. Student assessment** | |
| **a- Assessment methods** | - Weekly sheet exercises at class room.<br>- Quizzes.<br>- Labs experiments and case study for more demonstration.<br>- Mid-term and final exams. |
| **b- Assessment schedule** | - Exercise sheet/Lab assignment: Weekly<br>- Quiz 1: Week no 4<br>- Mid-term exam: Week no 8<br>- Quiz 2: Week no 12<br>- Lab exam: Week no 15<br>- Final-term examination: Week no 16 |
| c- **Weighting of assessment** | - Class tutorial and quizzes: 10%<br>- Mid-term examination: 15 %<br>- Case study: 5 %<br>- Final-term examination: 70 %<br>Total 100 % |
| 8. **List of text books and references** | |
| **a- Course notes** | - There are lecture notes prepared in the form of a book authorized by the department. |
| **b- Text books** | - Neil H. E. Weste, D. M. Harris, Integrated Circuit Design, 4th ed, Pearson Higher Education, 2011, ISBN: 978-0-321-69694-6. |
| **c- Recommended books** | [1] E. Brunvand, Digital VLSI Chip Design With Cadence and Synopsys CAD Tools, 1st ed. Reading, MA: Addison-Wesley, 2009.<br>[2] Ayers, J. E. Digital integrated circuits: analysis and design, CRC Press, 2004.<br>[3] R. J. Baker, H. W. Li, and D. E. Boyce, CMOS, Circuit Design, Layout, and Simulation, New York: IEEE Press, 1998. |
| **d- Periodicals, Web sites, etc.** | www.mrc.uidaho.edu/vlsi/cad_free.html,<br>www.webopedia.com/TERM/V/VLSI.html<br>www.inf.ufrgs.br/vlsisoclsi<br>www.epfl.ch/LSI2001/teaching/.../toc.html<br>www.ce.rit.edu/people/lukowiak/eecc630/Syllabus.pdf |

## Course contents - ILOs Matrix

| Content topics | Week | A- Knowledge & understanding | B- Intellectual skills | C- Professional and practical skills | D- General and transferable skills |
|---|---|---|---|---|---|
| Introduction - MOS transistor theory - Modeling of transistor using SPICE | 1-3 | A.1, A.3 | B.1, B.5 | C.6 | D.2,D.3,D.4, D.6, D.7 |
| fabrication of circuits MOS - Inverter static characteristics - Inverter dynamic characteristics | 4-5 | A.4, A.8 | B.5, B.6 | C.3, C.6 | D.3, D.6, D.7 |
| Combinational MOS | 6-9 | A.1, A.3 | B.5, B.6 | C.2, C.6 | D.3, D.6, D.7 |

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| logic - Sequential MOS logic circuits. | | | | | |
| MOS semiconductor memories - Description component and analysis | 10-12 | A.3, A.19 | B.1 | C.3 | D.3, D.6, D.7 |
| Interaction with matter Ion Implementation. | 13-14 | A.1, A.8 | | C.2, C.3 | D.3, D.6, D.7 |

## Teaching and learning methods - ILOs Matrix

| Teaching and learning methods | A. Knowledge & understanding | B. Intellectual skills | C. Professional & practical skills | D. General & transferable skills |
|---|---|---|---|---|
| Lectures | A.1, A.3, A.4, A.8, A.19 | B.1, B.5, B.6 | C.2, C.3, C.6 | D.3 |
| Tutorials | A.1, A.3, A.8, A.19 | B.1, B.5, B.6 | C.2, C.3 | D.3,D.6,D.7 |
| Exercises | A.1, A.3, A.4, A.8, A.19 | B.1, B.5, B.6 | C.2, C.3 | D.6,D.7 |
| Lab | A.4 | B.1, B.5, B.6 | C.2, C.3, C.6 | D.2,D.3,D.4,D.6,D.7 |

## Assessment methods - ILOs Matrix

| Assessment methods | A. Knowledge & understanding | B. Intellectual skills | C. Professional & practical skills | D. General & transferable skills |
|---|---|---|---|---|
| Weekly sheet exercises | A.1, A.3, A.4, A.8, A.23 | B.1, B.5, B.6 | C.2, C.3 | D.6,D.7 |
| Reports | A.1, A.3, A.4, A.8, A.19 | B.1, B.5, B.6 | C.2, C.3 | D.6,D.7 |
| Quizzes | A.1, A.3, A.4, A.8, A.19 | B.1, B.5, B.6 | C.2, C.3 | D.2,D.4,D.6 |
| Lab exam | A.4 | B.1, B.5, B.6 | C.2, C.3, C.6 | D.2,D.4,D.6 |
| Mid-term and final written exams | A.1, A.3, A.4, A.8, A.19 | B.1, B.5, B.6 | C.2, C.3 | D.6 |

Authorized from department board at 15/05/2016
Authorized from college board at 05/06/2016

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