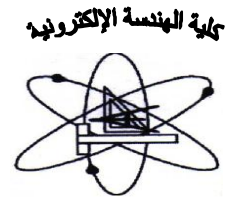


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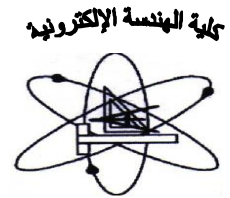


Department offering the program: Electronics and Electrical Communications Engineering
Department offering the course: Electronics and Electrical Communications Engineering

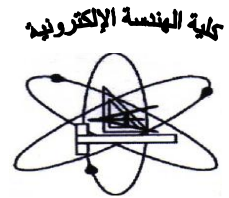
Course Specification

1. Course Basic Information		
Code ECE 212 Department requirement	Title: Very Large Scale Integrated Circuit	Academic year: 2015-2016 Level (2) – Semester (1st)
Field: Basic Eng. Science	Teaching hours: Lecture [2] Tutorial [1] Lab [0]	

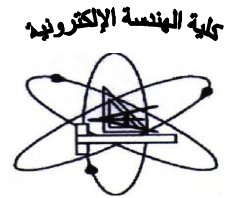
2. Course Objectives	<ol style="list-style-type: none"> To provide students with the basics of MOS transistor theory and modeling using SPICE. To give students a comprehensive study for the principles and techniques of modern VLSI systems design. To develop the student's skills to analyze and design the VLSI technology. To teach students the analysis of combinational MOS logic circuits, sequential MOS logic circuits, and MOS semiconductor memories. To equip students with integrated circuits different fabrication methods.
3. Intended learning outcomes: ARS	Course ILOs
A- Knowledge and understanding	<p>A.1 Explain concepts and theories of mathematics and science, appropriate to very large scale integrated circuit.</p> <p>A.3 Describe characteristics of engineering materials related to very large scale integrated circuit.</p> <p>A.4 Demonstrate principles of design including elements design, process and/or a system related to very large scale integrated circuit.</p> <p>A.8 Describe current engineering technologies as related to very large scale integrated circuit.</p> <p>A.19 Explain methods of fabrication of integrated circuits.</p>
	<p>A.1.1 Explain MOS transistors concepts and theories.</p> <p>A.1.2 Explain VLSI layout concepts.</p> <p>A.1.3 Explain the concepts of inverter, static and dynamic logic, and memory circuits.</p> <p>A.3.1 Describe characteristics of materials used in integrated circuit fabrication.</p> <p>A.4.1 Demonstrate design principles of combinational and sequential MOS logic circuits.</p> <p>A.4.2 Demonstrate design principles of MOS semiconductor memories.</p> <p>A.8.1 Describe current engineering technologies related to MOS logic circuits.</p> <p>A.8.2 Describe current engineering technologies related to MOS semiconductor memories.</p> <p>A.8.2 Describe current engineering technologies related to integrated circuits fabrication.</p> <p>A.19.1 Describe methods of fabrication of MOS semiconductor memories.</p> <p>A.19.1 Describe methods of fabrication of combinational and sequential MOS logic circuits.</p>



<p>B- Intellectual skills</p>	<p>B.1 Select appropriate mathematical and computer-based methods for modeling and analyzing problems.</p> <p>B.5 Assess and evaluate the characteristics and performance of components, systems and processes.</p> <p>B.6 Investigate the failure of components, systems, and processes.</p>	<p>B.1.1 Select appropriate mathematical methods for analyzing MOS transistor performance.</p> <p>B.1.2 Select appropriate computer-based methods for modeling MOS transistor using SPICE.</p> <p>B.5.1 Assess the characteristics of static and dynamic inverters.</p> <p>B.5.2 Evaluate the performance MOS transistor.</p> <p>B.6.1 Investigate the failure of MOS semiconductor memories.</p>
<p>C- Professional skills</p>	<p>C.2 Professionally merges the engineering knowledge, understanding, and feedback to improve design, products and/or services.</p> <p>C.3 Create and/or re-design a process, component or system, and carry out specialized engineering designs.</p> <p>C.6 Use a wide range of analytical tools, techniques, and software packages pertaining to very large scale integrated circuits and develop required computer programs.</p>	<p>C.2.1 Professionally merges the engineering knowledge and understanding to improve MOS semiconductor memories design.</p> <p>C.3.1 Create combinational and sequential MOS logic circuits.</p> <p>C.3.2 Create MOS semiconductor memories circuits.</p> <p>C.3.3 Create layout designs for different integrated circuits.</p> <p>C.6.1 Use SPICE analytical tool for modeling MOS transistors.</p> <p>C.6.2 Use the appropriate software package to make VLSI layout.</p>
<p>D- General skills</p>	<p>D.2. Work in stressful environment and within constraints.</p> <p>D.3 Communicate effectively.</p> <p>D.4 Demonstrate efficient IT capabilities.</p> <p>D.6 Effectively manages tasks, time, and resources.</p>	<p>D.2.1 Work in stressful environment and within constraints in understanding Modeling of transistor using SPICE.</p> <p>D.3.1 Communicate effectively, in class room and lab time with his colleagues and staff members.</p> <p>D.4.1 Demonstrate efficient IT capabilities with using SPICE.</p> <p>D.6.1 Effectively manages tasks, time, and resources in the Lab assignments, and exams.</p>



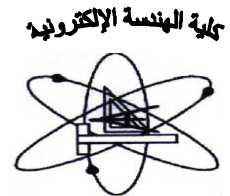
D.7. Search for information and engage in life-long self learning discipline.	D.7. 1 Search for information and engage in life-long self learning in modeling of MOS transistor and fabrication of MOS circuits. D.7. 2 Search for information and engage in life-long self learning relevant to integrated circuits analysis and design.
4. Course contents	<p><u>MOSFET and Fabrication Technology</u>, The pass transistor, NMOS, <u>MOS Inverter</u> and BiCMOS. Fabrication of NMOS Device/ Transistor Fabrication of CMOS Devices, <u>n-Well Process</u>, <u>P-well Processing Steps</u> Twin-Tub Processing. Stick diagrams. NMOS design style, CMOS-design style. Design rules and layout, Lambda-based design rules. Double metal MOS process rules, CMOS lambda-based design rules, 2μm double metal, double poly. CMOS / BiCMOS rules, Layout diagrams, Symbolic diagrams - translation to mask form. Transmission gates, Gate (restoring) logic. The inverter, Two-input NMOS, CMOS and BiCMOS Nand gates, Two-input nMOS, CMOS and BiCMOS Nor gates. Pseudo-nMOS logic, Dynamic CMOS logic, Clocked CMOS (CZMOS) logic, CMOS domino logic, n-p CMOS logic, A parity generator, Bus arbitration iogic for n-line bus. Multiplexers (data selectors), A general logic function block, A four-line Gray code to binary code converter, The programmable logic array (PLA), Two-phase clocking, Charge storage, Dynamic register element, A dynamic shift register. Illustration of the design process computational elements, Some observations on the design process, Design of a 4-bit adder, Implementing ALU functions with an adder, The Manchester carry-chain. Some CMOS design projects, CMOS project 1 - an incrementer/decrementer: MOS project 2 - left/right shift serial/para register: CMOS project 3 - a comparator for two n-bit numbers: CMOS/BiCMOS project 4 - a two-phase non-overlapping clock generator with buffered output on both phases: CMOS project 5 - design of a latch - an event-driven latch element for EDL systems.</p> <p><u>ترانزستور تأثير المجال ذو البوابة المعزولة وطرق تصنيعه- عاكس ترانزستور تأثير المجال ذو البوابة المعزولة - دوائر العاكس المتكامل وثنائي القطبية- التصنيع باستخدام البئر الالكترونى و التصنيع باستخدام البئر الفجوى- الرسم التخطيطى للترانزستور- قواعد الرسم التخطيطى للتصميم- التحويل لصورة القناع- بوابات النقل - البوابات المنطقية- دوائر الناند و النور- المولد الازدواجى- الدماجات - تحويلات الجراى كود- مصفوفات البوابات المبرمجة- المسجلات الديناميكية- تصميم العناصر الحسابية المجمعمة- تصميم الجامع - تصميم الوحدات الحاسبة و المنطقية- مشاريع تطبيقية.</u></p>
5. Teaching and learning methods	<ul style="list-style-type: none"> - Lectures - Tutorials - Labs and case studies - Research assignments
6. Teaching and learning methods for disable students	<ul style="list-style-type: none"> - Assign a portion of the office hours for those students. - Arrange meetings for more discussion and declaration. - Repeat the explanation of some of the material and tutorials. - Assign a teaching assistance to follow up the performance of this group



	of students.
7. Student assessment	
a- Assessment methods	- Weekly sheet exercises at class room. - Quizzes. - Labs experiments and case study for more demonstration. - Mid-term and final exams.
b- Assessment schedule	- Exercise sheet/Lab assignment: Weekly - Quiz 1: Week <u>no</u> 4 - Mid-term exam: Week <u>no</u> 8 - Quiz 2: Week <u>no</u> 12 - Lab exam: Week <u>no</u> 15 - Final-term examination: Week <u>no</u> 16
c- Weighting of assessment	- Class tutorial and quizzes: 10% - Mid-term examination: 15 % - Case study: 5 % - Final-term examination: 70 % Total <u>100 %</u>
8. List of text books and references	
a- Course notes	- There are lecture notes prepared in the form of a book authorized by the department.
b- Text books	- Neil H. E. Weste, D. M. Harris, Integrated Circuit Design, 4 th ed, Pearson Higher Education, 2011, ISBN: 978-0-321-69694-6.
c- Recommended books	[1] E. Brunvand, Digital VLSI Chip Design With Cadence and Synopsys CAD Tools, 1st ed. Reading, MA: Addison-Wesley, 2009. [2] Ayers, J. E. Digital integrated circuits: analysis and design, CRC Press, 2004. [3] R. J. Baker, H. W. Li, and D. E. Boyce, CMOS, Circuit Design, Layout, and Simulation, New York: IEEE Press, 1998.
d- Periodicals, Web sites, etc.	www.mrc.uidaho.edu/vlsi/cad_free.html , www.webopedia.com/TERM/V/VLSI.html www.inf.ufrgs.br/vlisisoclsi www.epfl.ch/LSI2001/teaching/.../toc.html www.ce.rit.edu/people/lukowiak/eccc630/Syllabus.pdf

Course contents - ILOs Matrix

Content topics	Week	A- Knowledge & understanding	B- Intellectual skills	C- Professional and practical skills	D- General and transferable skills
Introduction - MOS transistor theory - Modeling of transistor using SPICE	1-3	A.1, A.3	B.1, B.5	C.6	D.2,D.3,D.4, D.6, D.7
fabrication of circuits MOS - Inverter static characteristics - Inverter dynamic characteristics	4-5	A.4, A.8	B.5, B.6	C.3, C.6	D.3, D.6, D.7
Combinational MOS	6-9	A.1, A.3	B.5, B.6	C.2, C.6	D.3, D.6, D.7



logic - Sequential MOS logic circuits.					
MOS semiconductor memories - Description component and analysis	10-12	A.3, A.19	B.1	C.3	D.3, D.6, D.7
Interaction with matter Ion Implementation.	13-14	A.1, A.8		C.2, C.3	D.3, D.6, D.7

Teaching and learning methods - ILOs Matrix

Teaching and learning methods	A. Knowledge & understanding	B. Intellectual skills	C. Professional & practical skills	D. General & transferable skills
Lectures	A.1, A.3, A.4, A.8, A.19	B.1, B.5, B.6	C.2, C.3, C.6	D.3
Tutorials	A.1, A.3, A.8, A.19	B.1, B.5, B.6	C.2, C.3	D.3, D.6, D.7
Exercises	A.1, A.3, A.4, A.8, A.19	B.1, B.5, B.6	C.2, C.3	D.6, D.7
Lab	A.4	B.1, B.5, B.6	C.2, C.3, C.6	D.2, D.3, D.4, D.6, D.7

Assessment methods - ILOs Matrix

Assessment methods	A. Knowledge & understanding	B. Intellectual skills	C. Professional & practical skills	D. General & transferable skills
Weekly sheet exercises	A.1, A.3, A.4, A.8, A.23	B.1, B.5, B.6	C.2, C.3	D.6, D.7
Reports	A.1, A.3, A.4, A.8, A.19	B.1, B.5, B.6	C.2, C.3	D.6, D.7
Quizzes	A.1, A.3, A.4, A.8, A.19	B.1, B.5, B.6	C.2, C.3	D.2, D.4, D.6
Lab exam	A.4	B.1, B.5, B.6	C.2, C.3, C.6	D.2, D.4, D.6
Mid-term and final written exams	A.1, A.3, A.4, A.8, A.19	B.1, B.5, B.6	C.2, C.3	D.6

Authorized from department board at 15/05/2016
Authorized from college board at 05/06/2016

Course coordinator:
Prof. Abd El-Naser A. Mohamed

Head of Department:
Prof. Fathi El-Sayed Abd El-Samie



جامعة المنوفية
كلية الهندسة الإلكترونية
قسم هندسة الاتصالات والكهربية

